

Section Number: \_\_\_\_\_

Name: \_\_\_\_\_

## Pre-Lab for Lab 5: From Boolean Function to Silicon

Fall 2022

1. Select a partner Partner name \_\_\_\_\_
2. Select either a NAND gate or a NOR gate, your partner should select the other  
Gate you selected \_\_\_\_\_
3. Select one of the following Boolean Functions to use in this experiment
  - $Y1 = ABC + \overline{A}BC + A\overline{B}C$
  - $Y2 = \overline{A}BC + A\overline{B}C + \overline{A}B\overline{C}$
  - $Y3 = (\overline{A} + B + C)(A + \overline{B} + C)(A + B + \overline{C})$
  - $Y4 = (\overline{A} + \overline{B} + C)(A + \overline{B} + \overline{C})(\overline{A} + B + \overline{C})$Function selected \_\_\_\_\_
4. Draw a stick diagram for your inverter and the other gate you selected in consultation with your lab partner. You should be guided by this stick diagram when you do the layout of your circuit. Consider how fingers and multipliers will help in the design.
5. Create a floorplan of the Boolean function that you selected. The floorplan should show the input and output pin placements and the relative location of the gates. Consider the stick diagram when creating the floorplan and modify the stick diagram if necessary to be compatible with your floorplan. When creating a floorplan of your layout, it is often convenient to have VDD and VSS busses running horizontal with gates placed between these two busses. To facilitate direct placement of gates in your layout, it would be good to have you and your partner to agree on the spacing between the VDD and VSS busses. It is also common practice to bring all inputs into a gate on the left side in M1 and have all outputs exit on the right side in M1 as well.
6. Attach proof that demonstrates the correctness of the gate level Boolean function of step 3. This can be done by hand by applying all 8 possible inputs and building a truth table for your circuit. Alternatively, you can use any other tool of your choice to build the truth table. Compare the truth table of your implementation with the truth table of the function assigned to you.
7. At the start of the lab, you will enter the top level schematic in Cadence and then test it by applying A, B, and C waveforms. What would those input stimuli be in order to exercise all combinations of the inputs? Draw a simple figure that shows the pulse width, period, etc., of each input waveform. What output waveform do you expect?